DIP COATING PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon Sheet Task of the Low-Cost Silicon Solar Array Project

Quarterly Report No. 2

by

J. D. Heaps, R. B. Maciolek, W. B. Harrison, H. A. Wolner, G. Hendrickson and L. D. Nelson

Period Covered: 12/19/75 - 3/18/76

Published March 22, 1976

Honeywell Corporate Research Center
10701 Lyndale Avenue South
Bloomington, Minnesota 55420

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

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ABSTRACT

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon.

To date, an experimental dip-coating facility has been constructed. Using this facility, relatively thin (~ 1 mm) mullite and alumina substrates have been successfully dip-coated with 2.5 - 3.0 ohm-cm, p-type silicon with areas of ~20 cm^2. The thickness and grain size of these coatings are influenced by the temperature of the melt and the rate at which the substrate is pulled from the melt. One mullite substrate had dendrite-like crystallites of the order of 1 mm wide and 1 to 2 cm long. Their axes were aligned along the direction of pulling.

A large variety of substrate materials have been purchased or developed enabling the program to commence a substrate definition evaluation.

Due to the insulating nature of the substrate, the bottom layer of the p-n junction may have to be made via the top surface. The feasibility of accomplishing this has been demonstrated using single crystal wafers.

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INTRODUCTION AND SUMMARY OF RESULTS

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating inexpensive ceramic substrates with a thin layer of large grain polycrystalline silicon. The dip-coating methods to be developed are to be directed toward a minimum-cost process with the objective of producing solar cells with a terrestial conversion efficiency of 10 percent or greater.

Previous to this program the Honeywell Corporate Research Center experimentally demonstrated that silicon coatings could be applied to carbonized ceramic substrates by immersing them into molten silicon and subsequently removing them at a pulling rate of ~1 cm/second. Layers resulting from this coating technique had growth-parameter-dependent thicknesses ranging from 25 to 100 micrometers, with crystalline grains substantially larger than the layer thickness.

This work is being continued under this contract program. To date, a summary of the progress of this program includes:

1. An experimental dip-coating facility has been designed, constructed, tested and modified as required. This facility has considerable research flexibility and will be used to study growth parameters for preparing silicon coatings with optimum grain sizes.

2. A JPL design review of this facility was performed as per program plan.

3. A Standard Operation Procedure document describing the operation of the dip-coating facility was prepared and submitted to JPL as per program plan.

4. Mullite and alumina substrates have been dip-coated with p-type silicon using this facility. These 2.5 - 3.0 ohm-cm coatings

have areas of approximately 20 cm^2 and thicknesses ranging from ~12 to 125 μmeters. The variations in the thicknesses of these coatings purposefully resulted from varying such growth parameters as pulling rate and melt temperature. One substrate had dendrites in the microstructure of its 45 meter thick coating that were feathery in appearance and typically 0.5 - 1.0 mm wide and 1-2 cm in length. A diffractometric analysis of the crystallographic surface texture of the coating showed a 1,0,0 orientation.

5. Honeywell's Ceramic Center has fabricated or purchased a sufficient variety of ceramic substrate materials to enable the Research Center to commence an evaluation directed toward substrate definition.

6. A satisfactory bottom and top layer solar cell electroding technique has been established using single crystal silicon wafers with p-n junctions.

As this program is continued, its efforts will be directed toward the remaining major tasks:

1. Definition of an inexpensive ceramic substrate material whose properties are compatible with silicon and the dip-coating process.

2. Development of a substrate carbonization technique.

3 Characterization of the optimum dip-coating growth parameters to maximize grain size and minimize individual crystallite dislocation density.

4. Characterization of the physical and electrical properties of the silicon coatings.

5. Evaluation of solar cells fabricated from the silicon coatings.

TECHNICAL DISCUSSION

EXPERIMENTAL DIP-COATING FACILITY

During this reporting period, the experimental dip-coating facility, discussed in detail in the 1st Quarterly Report, was completed, tested and modified as required. As shown in Photo No. 1, the facility consists of the following three major components:

1. The main frame of the dip-coating assembly consisting of the following major parts:

   - a water-cooled melt chamber with a viewing port. This assembly permits evacuation of the chamber and a subsequent purging with argon gas.

   - a gas lock and pulling rod assembly which enables the operator to install and remove numerous substrates during the course of a day's operation.

   - a programmable dip-pull mechanism.

   - a control panel for operating the facility.

   - a Honeywell Dialatrol temperature controller

   - a Honeywell Electronic Type 125 two-pen chart recorder for recording pulling rates and melt temperature.

   - an adjustable gas flowmeter

   - a water flow failure shut-down switch

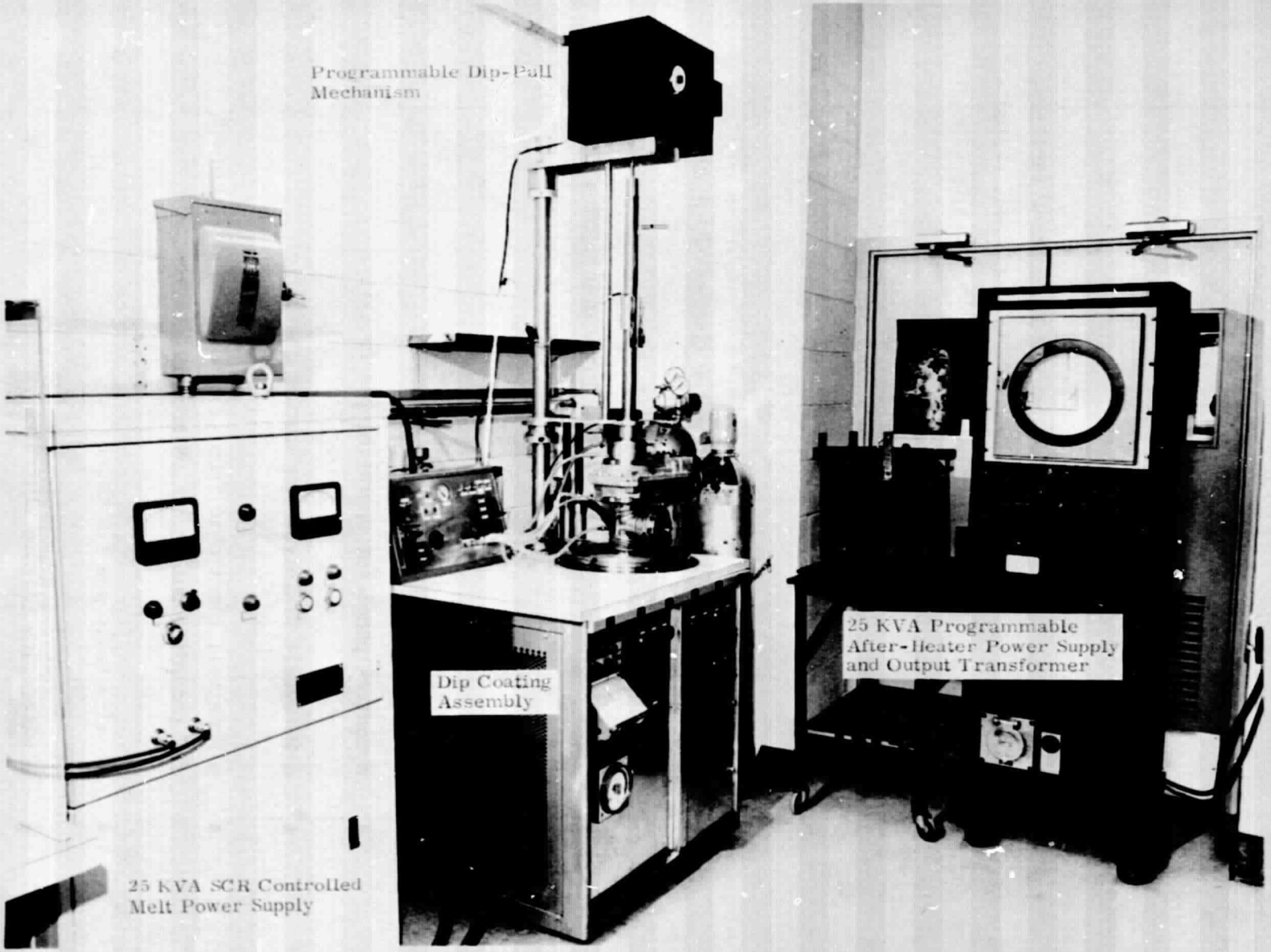

Photo No. 1- Experimental Dip-Coating Facility

2. A 25KVA, SCR controlled melt heater power supply.

3. A 25 KVA "After-Heater" power supply consisting of the following:

   - a programmable cam temperature controller with a circular chart recorder
   - a Honeywell Electrodyne motor-driven multiple variac power supply
   - a 30 KVA step-down transformer for matching the impedance of the "After-Heater."

The original design for installing the "After-Heater" directly above the silicon melt had to be modified to overcome a possible graphite crucible holder breakage problem during the facility shut-down operation. To ensure that the graphite crucible holder will not be broken when the quartz crucible expands and breaks during the solidification of the silicon melt, the quartz crucible containing the molten silicon is raised out of its graphite holder at shut-down time. This makes it necessary to externally reposition the "After-Heater" by an externally controlled lever. As such, to date the "After-Heater" assembly has not yet been installed. All parts and components of this assembly have been constructed and are presently being added to the facility.

On February 27, the design of the dip-coating facility was reviewed by the program's contract monitor, Dr. Martin H. Leipold. At that time he was presented with a copy of a "Standard Operation Procedure" document describing the operation of the facility.

DIP-COATING RESULTS

Three mullite substrates and one 97% alumina substrate were dip-coated with p-type silicon. The mullite substrates were fabricated at Honeywell's Ceramic Center by rolling, drying and firing a wet plastic formulation. Details of this process will be given in a later section of this report.

The substrates used were ~ 6 cm x 5 cm in area and ~ 1 mm thick. They were immersed ~4 cm into the molten silicon thus producing silicon coatings of ~ 20 cm^2 in area. (See Photo No. 2) One surface of these substrates was coated with carbon by scrubbing ultra pure carbon over the surface and subsequently removing all surplus powder. Both the mullite and alumina substrates proved to be thermally compatible with the dip-coating process by withstanding the thermal shock of being immersed into the molten silicon with no visible sign of cracking. The alumina substrate was not cleaned and fired before dip-coating and therefore produced only a spotty coating.

The character of each of these coatings varied, as expected, with the temperature of the melt and the pulling rates employed. Table No. 1 lists data pertinent to the growth parameters used in coating the aforementioned substrates.

Metallurgical characterization of the samples was done by visual inspection, to assess structural integrity, and metallographic examination of sectioned and etched specimens by optical microscopy to measure film thickness and grain size. The etchant used to delineate grain boundaries was dilute CP_4.

All the films shown in Photo No. 2 were prepared on mullite substrates. The silicon covered only the side of the substrate that had been coated with carbon. The surfaces of the films appeared bright and shiny to the eye. No cracks were observed in any of the substrates or films. The top edge of each film had a slightly thicker ridge running across it. Excellent adherence of the films to the substrates was noted in the course of handling. The microstructures of all the films were dendritic in nature, with the size of the dendrites being dependent on the growth parameters, pulling rate and melt temperature.

Substrate coating No. 1 (See Photo No. 2) was pulled at the slowest rate 0.12 cm/sec at a melt temperature of 1434°C. The surface of the sample was covered with gentle ripples running across the film from top to bottom.

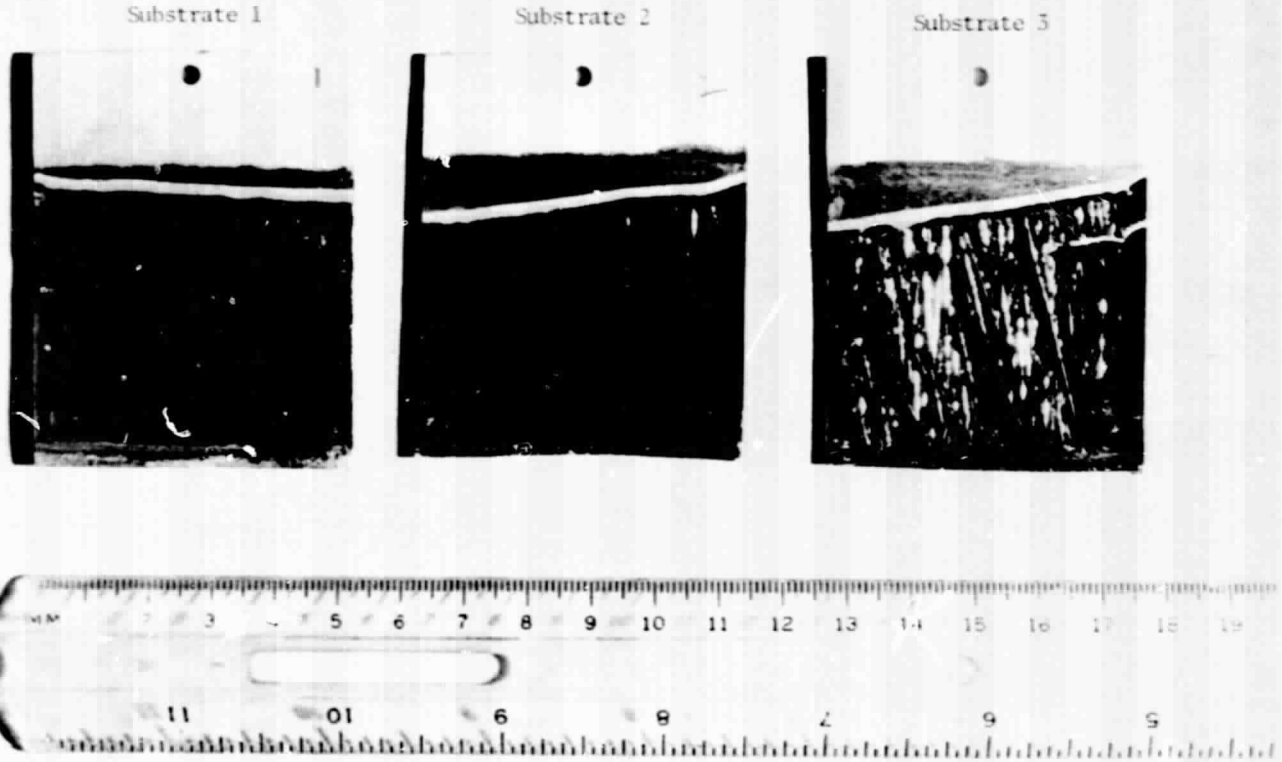

Photo No. 2 Dip-Coated Mullite Substrates

TABLE I. DIP-COATED SAMPLE GROWTH DATA

SUBSTRATE NO.	SUBSTRATE MATERIAL	MELT TEMP. (°C)	DIP RATE (cm/sec)	SOAK TIME (sec)	PULL RATE (cm/sec)
1	Rolled Mullite	1434	Irregular	60	0.12
2	Rolled Mullite	1426	0.5	60	0.33
3	Rolled Mullite	1410	0.5	90	0.33
4	97% alumina	1444	0.5	45	0.1

These were caused by operating the pulling motor controller at too low a level causing jerkiness in the motor. At faster pulling rates these ripples were eliminated on subsequent coatings.

The dendrites in the microstructure of substrate coating No. 1 were feathery in appearance (See Photo No. 3) and typically 1 mm wide and 1-2 cm long. The axes being aligned with the pulling direction. X-ray diffraction showed that the crystallographic surface texture of the film was 1, 0, 0. The film measured 45 μmeters in thickness.

Substrate coating No. 2 (See Photo No. 2) was pulled at 0.33 cm/sec from a melt at 1426°C. Its surface appeared quite smooth. The dendrites in its microstructure were more "tree like" in appearance and were ~50 μmeters (2 mils) wide and 250 μmeters (10 mils) long. The long axes were aligned in the direction of pulling. The film thickness was 12.5 μmeters (.5 mils).

Substrate coating No. 3 (See Photo No. 2) was pulled at 0.33 cm/sec from the coolest melt, 1410° C. The microstructure of this sample was dominated by coarse dendrites emanating from the leading edge of the film. The needle-like main branch of these dendrites were often 1 mm wide and 1-2 cm. long. The surface was not smooth due to the varying thicknesses of these dendrites. Film thickness ranged from 25 μmeters (1 mil) to 150 μmeters (6 mils).

The dendrite nature of the films is indicative that supercooling of the melt existed in all cases before solidification. The various dendritic morphologies reflect the degree of supercooling. Most encouraging is the fact that in all the films there was evidence that the first solidification occurred at the leading edge of the film. This suggested that under the proper conditions nucleation and growth could be controlled and both grain size and quality be improved.

The slightly thicker ridge of material at the top of each film is a consequence of the manner in which pulling was started, i.e. it took a finite amount of time to reach the desired pulling rate and the film grew thicker at the slower rates.

3.75X

7.5X

Photo No. 3 Crystalline Grains in Quarter Section of Substrate No. 1

The silicon charge was doped to produce a single crystal with an impurity concentration of 5.6×10^{15} atoms/cm^3. This, as reported by J. C. Irwin (see Fig. 1) is the equivalent of 2.5 ohm-cm resistivity. Our measurements show this p-type sample to vary from 2.5 to 3.0 ohm-cm. This measurement prevailed irrespective of the orientation of the 4-point probe. A somewhat larger resistivity results from this doping level in previously grown CVD coatings with average crystallites of ~125 μmeters. Caution must be given to the resistivity measurement of the dip-coated sample, however, since it was based on measuring a thin wafer on an insulating base, SiC is an insulator, but can be a semiconductor when doped. Should the SiC base layer be a good conductor, a correction would have to be made which would increase the magnitude of this measured value. We choose to accept this ideal measurement since the SiC layer is so relatively thin compared to the silicon coating.

SOLAR CELL ELECTRODES

Honeywell's previous work (see Fig. 2) clearly shows that heavily doped (> 5×10^{19} atoms/cm^3) n-type polycrystalline silicon have essentially the same resistivity as comparable doped single-crystal silicon. One should therefore expect, that by using an optimized top layer contacting grid network, the ohmic series resistance (R_S) contributed by the top layer of solar cells fabricated from either single or polycrystalline silicon, for a given area, should, for the most part, be identical.

The p-type base layer R_S of a typical* 2 cm x 2 cm single crystal solar cell is ~3.75×10^{-2} ohms.

Since a dip-coated solar cell's insulating substrate requires contacting the base layer from the top surface by etching (or otherwise cutting) through the junction barrier, calculations reveal, that by alternately interlacing the base and top layer contacting grid lines, the dip-coated base layer R_S would be only 1.46 times that of the typical single crystal

* Typical defined as being n on p with a 3 ohm-cm base layer and a 3000Å junction depth using a 0.5 mm thick wafer. The top layer has parallel contacting grid lines 0.25 mm wide and 3.33 mm on center.

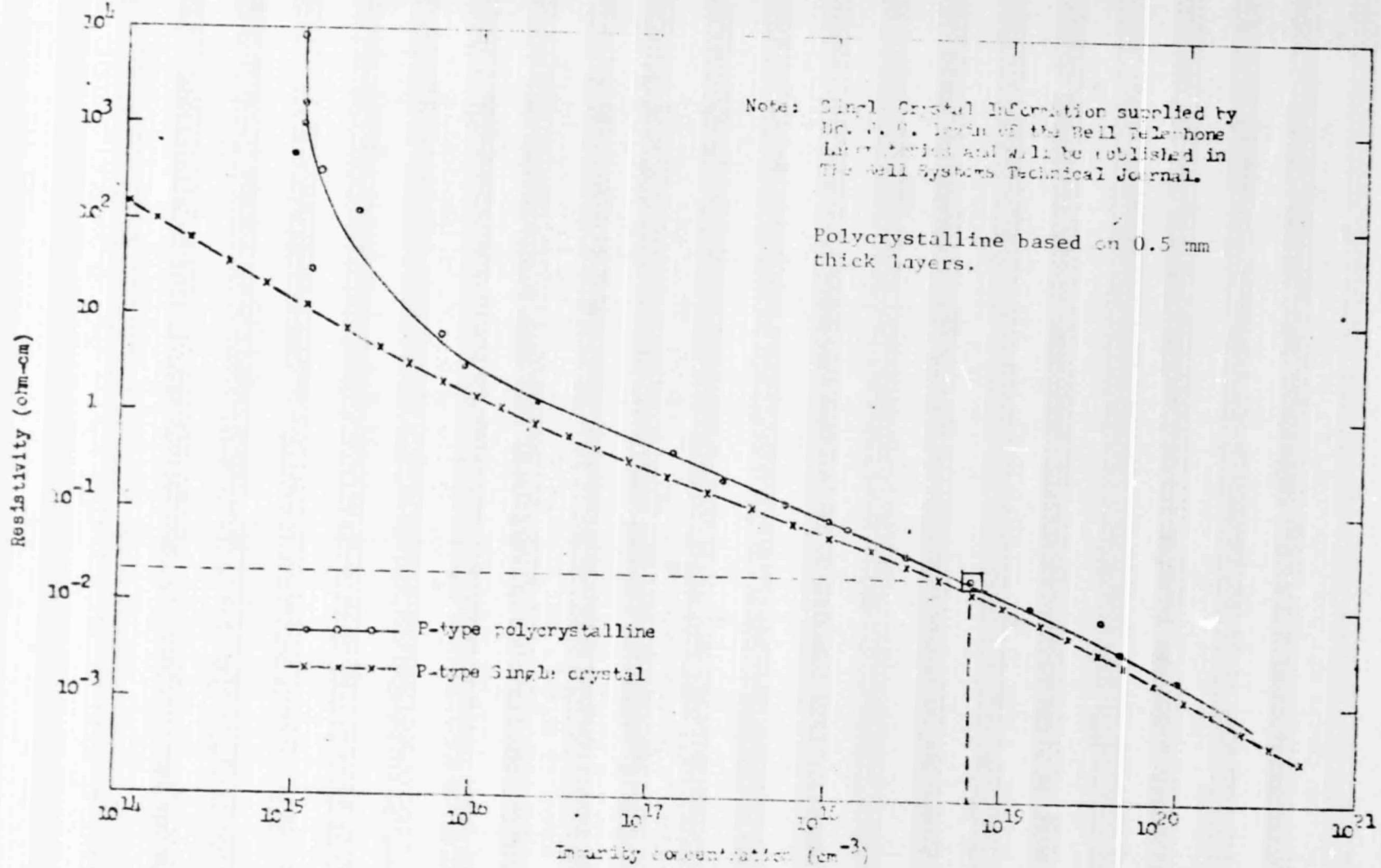

Figure 1 - COMPARISON OF P-TYPE POLYCRYSTALLINE RESISTIVITY WITH SINGLE CRYSTAL RESISTIVITY AT VARIOUS IMPURITY LEVELS

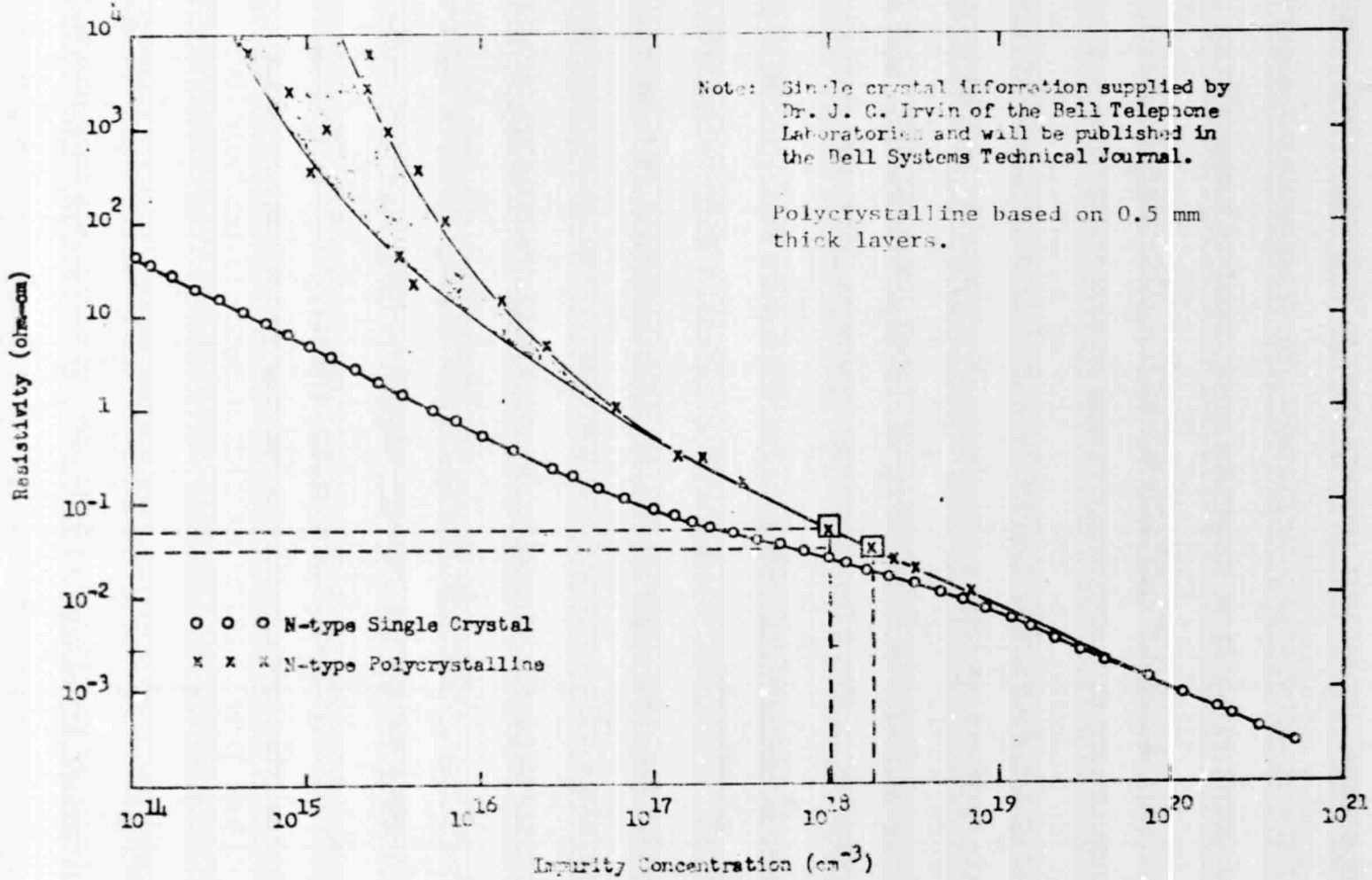

Figure 2 - COMPARISON OF N-TYPE POLYCRYSTALLINE RESISTIVITY WITH SINGLE CRYSTAL RESISTIVITY AT VARIOUS IMPURITY LEVELS

cell. Since the solar illuminated forward resistance of a 2 cm x 2 cm, 10% efficient single crystal cell is ~3.85 ohms, this additional base layer R_S is probably not significant.

The optimized top layer contacting grid network of a typical 2 cm x 2 cm cell occupies ~12% of the total area. By using the above-mentioned interlacing configuration for contacting the base layer of a dip-coated cell, it would increase this non-productive area to ~30% of the total area. Such a large non-productive area seems excessive and indicates that only when dip-coated solar cells have actually been fabricated and evaluated that properly optimized contacting networks can be worked out. For this reason we conclude, at this stage of our program, that it would be futile to design the necessary art work for contacting to our future dip-coated solar cells by photo resist or metal masking techniques. This conclusion is further supported by the fact that our initial dip-coated cells are unlikely to be entirely flat and would not accommodate sophisticated electrical contacting techniques.

For the present, single crystal and dip-coated solar cells will be electrically contacted in the following manner:

1. Following the junction diffusion, the grid pattern for contacting the base layer will be masked with 16 mil Teflon tape and the remaining unmasked area subsequently covered with a CP_4 acid resistant coating (Apiezon wax, etc.)

2. Once this coating has hardened, the Teflon tape will be removed and the exposed pattern etched through the junction to the base layer. (Due to the shallow junction depth, very little silicon need be removed.)

3. The acid resistant coating will then be removed and the wafer thoroughly cleaned.

4. 10-mil strips of Teflon tape will again be placed in the central region of this previously etched 16-mil wide base layer pattern. Additional 10-mil strips of tape will also be applied to form the

top layer contact pattern. A thin coating of a dissolvable substance (photo resist, lacquer, etc.) will be applied to the unmasked regions, and after drying the tape, once again removed.

5. Electroless nickel plating will then be applied to the exposed patterns.

6. The soluble coating will then be removed and the wafers cleaned and dipped into a solder pot to complete the contacting.

To date this technique has been successfully employed on single crystal silicon wafers with p-n junctions.

CERAMIC SUBSTRATE DEVELOPMENT

In addition to developing a material to be compatible with molten silicon, this portion of the program was spent examining several processing approaches, which could be scaled-up to square meter size substrates. These approaches include, rolling, casting, doctor blading and hot pressing. Rolling of a high plasticity, mullite material has been examined and substrates as large as 500 cm^2 have been formed and fired. Rolling and doctor blading of a calcium aluminate bound alumina material has also been shown to be feasible. Casting and doctor blading of a silica substrate has also been demonstrated. Hot pressing of fiberglass products into large 500 cm^2 sheets has also been accomplished.

Standard 25 cm^2 test samples for this program have been prepared or received from vendors as indicated in Table II. Each of these materials is discussed below.

Mullite: Mullite is an aluminum silicate compound ($3Al_2O_3 \cdot 2SiO_2$) which is available in many forms. The pure material has a melting point of about 1850°C, but up to 30% glassy phase is commonly found in this material which lowers the softing point. The thermal expansion and conductivity of mullite is about 5.0×10^{-6}/C and 3.5 Btu/hr-ft:°F respectively and its theoretical density is 3.26 gm/cc. The following four types of mullite have been obtained for this program.

TABLE NO. II SUBSTRATE MATERIAL STATUS

MATERIAL	TRADE NAME	SOURCE	FABRICATION PROCESS	FIRING TEMP.	STATUS
Mullite	MV-20	McDaniel Corp	Rolling	1640°C 20% glass	X
Mullite	MV-30	McDaniel Corp	Casting	-- 15% glass	X
Mullite	Fiberfrax	Carborundum	Hot Pressing	1400°C	X
Mullite		American Lava	Pressed		Due 4/1
Corderite	Alsimag 701	American Lava	(Purchased)	--	X
Corderite	A-3171	Du-Co	(samples)	--	
Alumina	Alsimag 614	American Lava	(Purchased)	-- 96% Al_2O_3	X
Alumina	Alsimag 798	American Lava	(Purchased)	-- 85% Al_2O_3	X
Polygranular SiO_2	GP-31	Glasrock Pdts. Inc.	Casting	1160°C 1400°C 1640°C	X X X
Calcium Aluminate	CA-25	Alcoa	Pressing & Rolling	60°C 1160°C 1640°C	X X X
Zirconia	Alsimag-475	American Lava			X
Sapphire	To be acquired				

X - samples on hand

1. Honeywell rolled MV-20
2. McDaniel casted MV-30
3. Honeywell hot pressed Fiberfrax
4. American Lava pressed material

McDaniel mullite composition MV-20 was procured in a plastic extrudable form. Test substrates (2" x 2½" x 1/16" thick) were produced by rolling the material out on a smooth, oiled surface and controlled drying and firing to 1640°C. After rolling, the sheet material was cut into oversized (2¼" x 2-3/4") coupons. The coupons were dried between flat plaster of Paris blocks for 20 hours at 60°C. They were then bisque fired on mullite sagger plates to 600°C and finally high temperature fired (on mullite) to 1640°C. The slight warpage which occurred during high temperature firing is attributed to non-uniform heating in the high convection gas-fired kiln. A total of 38, 2" x 2½" substrates have been produced. Several larger 3" x 5" substrates and 8" x 9" substrates were successfully prepared of this material by the rolling methods.

A second McDaniel mullite composition MV-30 was procured in fired tubular form. Eight (2" x 2½" x 3/16" thick) test coupons were cut from this material. The MV20 and MV30 materials typically contain 20 and 15% glassy phase after firing.

An additional one hundred 2" x 2" x 0.1" experimental pressed mullite substrates have also been ordered from American Lava Div of 3M Inc. Rigid sheets of mullite fibers have also been formed by pressing double or triple layers of Fiberfrax (0.05" thick Carborundum sheet) under a load at 1400°C. Flat very porous rigid sheets 0.04 to 0.06" thick with a density of 0.5 gm/cc. were formed by this process.

Alumina: Alumina substrates are the most common type of flat ceramic material used for electronic circuitry. Pure Al_2O_3 has a melting point of about 2000°C and a thermal expansion and conductivity of 6.7 to 10^{-6}/°C and 10.0 Btu/hr-ft-°F respectively. The theoretical density of this material is 3.98 gm/cc.

Two types of alumina substrates have been obtained for this program. One hundred pressed 96% and 85% alumina 2" x 2" x 0.05" plates have been procured from American Lava. These are designated as Alsimag 614 and 798, respectively. A third type of alumina has been fabricated at Honeywell by rolling, pressing and doctor blading of a calcium aluminate bound alumina material. Table III gives four compositions that have been formulated for Alcoa CA-25 calcium aluminate cement and tabular alumina filler. The consistency of the mixture was varied by addition of water based on the method of forming.

Smooth compress surfaces with no sticking were accomplished at 5,000 psi pressure. No apparent warpage occurred during firing. Rolled substrates had some surface roughness. Slight warpage occurred during high temperature firing. These materials were still somewhat porous but still had a density over 3.0 gm/cc.

Zircon: Zircon is a zirconia silicate ($ZRO_2 \cdot SiO_2$) compound with a melting point of 1530°C and theoretical density of 4.68 gm/cc. The thermal expansion and conductivity of this material is 6.0×10^{-6}°C. and 3.8 Btu/hr-ft-°F, respectively. One hundred pressed 2.0" x 2.0" x 0.1" substrates of Alsimag 475 have been procured from American Lava for this program.

Cordierite: Cordierite is a magnesium aluminum silicate ($2 M_5 0.2Al_2 0_3 \cdot 5SiO_2$) with a melting point of 1200°C, however, slightly different modifications may be as high as 1400°C. This material has a thermal expansion of 1.5×10^{-6}/°C.

Sample Cordierite substrates were obtained from the following two suppliers.

1. Minnesota Mining and Mfg. Co. (3M - Alsimag 701)
2. Du-Co Ceramics Co. (A-3171)

A specimen of each material was fired at 1500°C with the results shown in Photo No. 4. Both materials show leaching out of a lower melting constituent. The 3M material retains its shape, but the Du-Co material melted

TABLE III. HONEYWELL CERAMICS CENTER FORMULATION DATA

FORMULATION NO.	MATERIALS	PROPORTIONS % by Wt	WATER % by Wt	FORMING METHODS	DRYING 60°C	BISQUE FIRING 600°C	H.T. FIRING 1160°C	H.T. FIRING 1400°C	H.T. FIRING 1640°C
1	Alcoa CA-25	55	20	Casting	X				
	Tab. Al_2O_3-325	30							
	Tab. Al_2O_3-48	15							
2	Glasrock GP-31	100	20	Casting	X	X	X		
					X	X		X	
3	Glasrock GP-31	80	19	Casting	X	X	X		
	GP-71	20			X	X			X
4	Alcoa CA-25	15	10	Pressing	X	X	X		
	Tab. Al_2O_3-325	85							
5	Alcoa CA-25	15	12	Pressing	X	X	X		
	Tab Al_2O_3-325	70							
	Tab Al_2O_3 -48	15							
6	Alcoa CA-25	15	10	Pressing	X	X	X		
	Tab Al_2O_3-325	55			X	X			X
	Tab Al_2O_3-48	30	15½	Rolling	X	X	X		
					X	X			X
7	Carborundum "Fiberfrax"			H.T. Sinter				X	

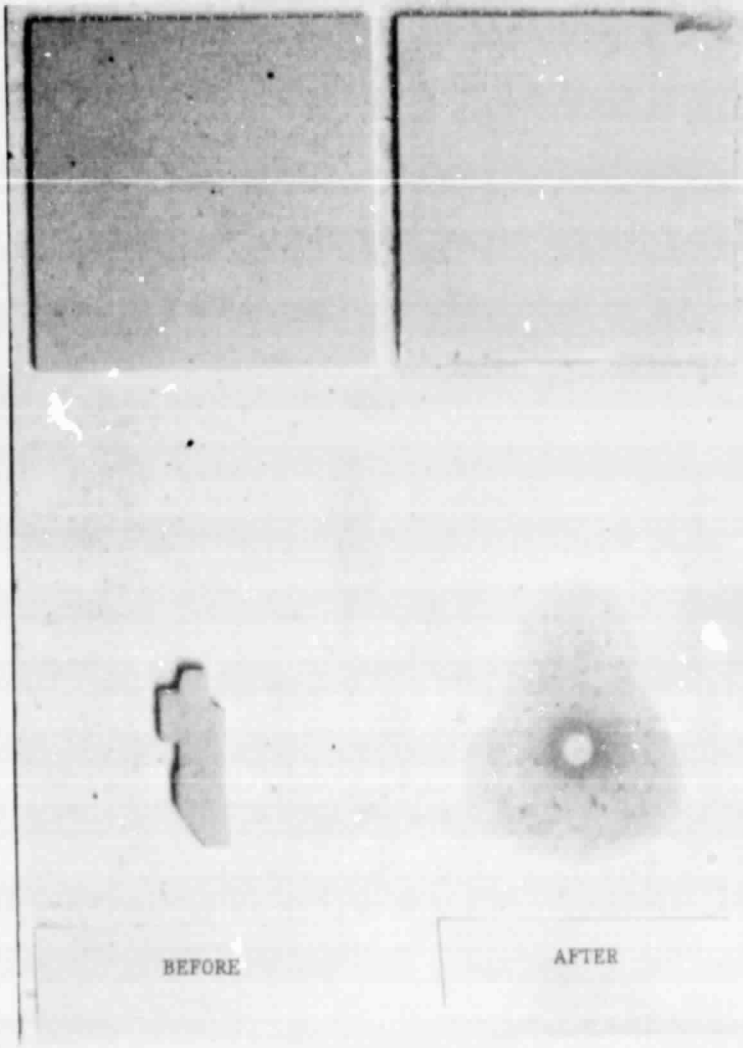

Photo No. 4 Cordierite Substrate Samples - 3M (Alsimag 701)
Upper and Du-Co (A3171)
Lower - Before and After Firing at 1500°C

completely. The Du-Co material will therefore not be evaluated for the silicon dip-coating application.

Silica: Silica in powdered form was procured from Glasrock Products. This Glasrock grade "I" material (99% SiO_2) was of two particle sizes designated GP31 (Fisher sieve 2.0) and GP 71 (Fisher series 4.5).

Two formulations were made (See Table III). In each case, a slip was prepared by high-shear mixing of the solid ingredients and water. The material was then cast on a flat porous substrate. The castings were dried at 60°C, bisque fired at 600°C and subsequently high temperature fired at either of two higher temperatures. (See Table III.)

A slight warpage of the cast sheets occurred after high temperature firing. This is attributed to a nonuniform particle size distribution through the sheet thickness. The fired substrates appear to have adequate structural strength for subsequent processing.

CONCLUSIONS AND RECOMMENDATIONS

As a result of our intial successful dip-coating results, the following conclusions are made:

1. That relatively thin (~ 1mm), larger area (~ 20 cm^2) flat mullite and alumina substrates have proven to be as thermally compatible with the dip-coating process as were the much smaller sections of ceramic tubing coated prior to this contract program.

2. That as previously demonstrated, the crystallization and layer thickness responds to and can be controlled by at least two growth parameters; namely pulling rate and melt temperature.

3. That the initial crystalline grains are dendritic in nature, but are nevertheless many times larger than the layer thickness. This more clearly demonstrates that a high degree of nucleation occurs from previously grown silicon. One can further conclude that such a nucleation process is likely to improve the chances for much larger crystallites as the area of the substrate is scaled up.

4. That the resistivity of the silicon coatings can apparently be predicted and controlled by the impurity doping methods associated with single crystal ingot growth.

5. That a multitude of variables are possible using this growth process, thus making it necessary to pursue a scientifically organized and methodic experimental approach to the research that is to follow.

During a recent meeting with the contract montitor, Dr. Leipold and Honeywell support personnel, further conclusions and recommendations were discussed and agreed upon. They are as follows:

1. That the Honeywell Ceramic Center has fabricated or purchased a sufficiently large variety of ceramic substrates to enable the Research Center to commence an evaluation directed toward substrate definition. Hence, no further substrate development should be undertaken until further dip-coating experiments provide the necessary feedback.

2. That further consideration should soon be given to alternate methods of coating carbon onto the substrate prior to dip-coating. Further, an effort should be made to minimize the variables introduced by the source of the carbon in these experiments.

3. That, if, carbon coatings and subsequent silicon coatings can be made to adhere to sapphire ribbons, that by coating these ribbons one should certainly reduce the number of impurity sources and thus improve the chances for identifying such contamination sources as those which may originate from the carbon coating, argon atmosphere, dip-coating facility parts, etc.

4. That fabrication of solar cell samples should proceed ahead of the plan schedule and should include making electrical contact to the bottom layer by the simplest method available.

PROJECTED THIRD QUARTER ACTIVITIES

In an effort to gain additional insight, a few additional dip-coating runs will immediately take place. A constructive research plan will then be developed to systematically cope with the many variables which are inherent to any totally new growth concept.

A systematic approach will commence designed toward the eventual characterization of optimized growth parameters which are compatible with the program's economic feasibility goals. Compromises will be given consideration.

Additional substrate materials will be evaluated and characterized with respect to their acceptability to the dip-coating process.

Additional techniques will be developed for carbonizing the ceramic substrate.

If possible, sapphire ribbons will be silicon coated in an effort to establish the influence of the substrate surface texture on crystallization or thereby determine the carbon coating's influence on crystallization. Using sapphire substrates will also establish a "best case" condition with respect to impurity contamination.

Cryogenic techniques will be investigated to determine their applicability as an additional electrical characterization method for identifying undesirable chemical impurities.

Techniques will be considered for determining the contribution, if any, of the silicon carbide film to the overall electrical conductivity of the silicon coating.

Finally, solar cell junctions will be evaluated and their conversion efficiencies compared with those of single crystal wafers, both of which will be fabricated together in a parallel effort.